In the Claims:

1. (Previously Presented) A semiconductor device, comprising:

a workpiece;

a first transistor formed in a first region of the workpiece, the first transistor having a first source, a first drain, and a first gate;

a second transistor formed in a second region of the workpiece, the second transistor having a second source, a second drain, and a second gate;

a first insulating layer disposed over at least the second source or the second drain of the second transistor; and

a second insulating layer disposed over at least the first source or the first drain of the first transistor and over the first insulating layer over the second source or the second drain of the second transistor, the second insulating layer comprising a different material than the first insulating layer, wherein the second insulating layer increases surface tension of a top surface of the first source or the first drain of the first transistor, and wherein the first insulating layer comprises a material that reduces surface tension of a top surface of the second source or the second drain of the second transistor.

2. (Cancelled)

3. (Previously Presented) The semiconductor device according to Claim 1, wherein the first transistor comprises a first channel region disposed beneath the first gate, wherein the second transistor comprises a second channel region disposed beneath the second gate, wherein the second insulating layer increases surface tension in the first channel region of the first transistor, and wherein the first insulating layer reduces surface tension in the second channel region of the second transistor.

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4. (Original) The semiconductor device according to Claim 1, wherein the first insulating layer comprises an oxide material and the second insulating layer comprises a nitride material or a carbon-containing material.

5. (Original) The semiconductor device according to Claim 4, wherein the first insulating layer comprises silicon dioxide or silicon oxynitride, and the second insulating layer comprises silicon nitride or silicon-carbon.

6. (Original) The semiconductor device according to Claim 4, wherein the first insulating layer comprises a thickness of about 400 Å or less, and wherein the second insulating layer comprises a thickness of about 850 Å or less.

7. (Original) The semiconductor device according to Claim 1, further comprising:

an interlevel dielectric (ILD) layer disposed over the first transistor and the second transistor;

a first contact formed within the ILD layer, the first contact making electrical contact to the first source or the first drain of the first transistor; and

a second contact formed within the ILD layer, the second contact making electrical contact to the second source or the second drain of the second transistor.

8. (Original) The semiconductor device according to Claim 7, wherein the ILD layer comprises a material etchable selective to the material of the second insulating layer.

9. (Original) The semiconductor device according to Claim 7, wherein the ILD layer comprises an oxide material, and wherein the second insulating layer comprises a nitride material or carbon-containing material.

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10. (Original) The semiconductor device according to Claim 7, further comprising a first bond pad disposed over the first contact, and a second bond pad disposed over the second contact.

11. (Original) The semiconductor device according to Claim 1, wherein the first region of the workpiece is proximate the second region of the workpiece, wherein the semiconductor device comprises a complimentary metal oxide semiconductor (CMOS) device, wherein the first transistor comprises an n channel metal oxide semiconductor transistor (NMOS) device, and wherein the second transistor comprises a p channel metal oxide semiconductor transistor (PMOS) device.

12. (Original) The semiconductor device according to Claim 11, wherein the first source and the first drain of the first transistor are N+ doped, and wherein the second source and the second drain of the second transistor are P+ doped.

13. (Original) The semiconductor device according to Claim 1, further comprising a silicide layer disposed over the first source, the first drain, and the first gate of the first transistor, and over the second source, the second drain, and the second gate of the second transistor.

14. (Original) A complimentary metal oxide semiconductor (CMOS) device, the CMOS device comprising:

a workpiece;

a first transistor formed in a first region of the workpiece, the first transistor comprising an n channel metal oxide semiconductor transistor (NMOS) device, the first transistor having a first source, a first drain, and a first gate;

a second transistor formed in a second region of the workpiece, the second transistor

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comprising a p channel metal oxide semiconductor transistor (PMOS) device, the second transistor having a second source, a second drain, and a second gate;

a surface tension-reducing layer disposed over at least the first source or the first drain of the first transistor;

a surface tension-inducing layer disposed over at least the first source or the first drain of the first transistor and over the surface tension-reducing layer over the second source or the second drain of the second transistor, the surface tension-inducing layer comprising a different material than the surface tension-reducing layer;

an interlevel dielectric (ILD) layer disposed over the first transistor and the second transistor;

a first contact formed within the ILD layer, the first contact making electrical contact to the first source or the first drain of the first transistor; and

a second contact formed within the ILD layer, the second contact making electrical contact to the second source or the second drain of the second transistor.

15. (Original) The semiconductor device according to Claim 14, wherein the surface tension-inducing layer increases surface tension of a top surface of the first source or the first drain of the first transistor, and wherein the surface tension-reducing layer comprises a material that reduces surface tension of a top surface of the second source or the second drain of the second transistor.

16. (Original) The semiconductor device according to Claim 15, wherein the first transistor comprises a first channel region disposed beneath the first gate, wherein the second transistor comprises a second channel region disposed beneath the second gate, wherein the surface tension-inducing layer increases surface tension in the first channel region of the first transistor,

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and wherein the surface tension-reducing layer reduces surface tension in the second channel region of the second transistor.

17. (Original) The semiconductor device according to Claim 14, wherein the surface tension-reducing layer comprises an oxide material and the surface tension-inducing layer comprises a nitride material or a carbon-containing material.

18. (Original) The semiconductor device according to Claim 17, wherein the surface tension-reducing layer comprises silicon dioxide or silicon oxynitride, and the surface tension-inducing layer comprises silicon nitride or silicon-carbon.

19. (Original) The semiconductor device according to Claim 14, wherein the surface tension-reducing layer comprises a thickness of about 50 Å to about 300 Å, and wherein the surface tension-inducing layer comprises a thickness of about 200 Å to about 700 Å.

20. (Original) The semiconductor device according to Claim 14, wherein the ILD layer comprises a material that is etchable selective to the material of the surface tension-inducing layer.

21. (Original) The semiconductor device according to Claim 20, wherein the ILD layer comprises an oxide material, and wherein the surface tension-inducing layer comprises a nitride material or a carbon-containing material.

22. (Original) The semiconductor device according to Claim 14, wherein the first source and the first drain of the first transistor are N+ doped, and wherein the second source and the second drain of the second transistor are P+ doped.

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23. (Original) The semiconductor device according to Claim 14, further comprising a silicide layer disposed over the first source, the first drain, and the first gate of the first transistor, and disposed over the second source, the second drain, and the second gate of the second transistor.

24. (Original) The semiconductor device according to Claim 14, further comprising a first bond pad disposed over the first contact, and a second bond pad disposed over the second contact.

25.-42. (Cancelled)

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